CLAIMS

Having thus described our invention in detail, what we claim is new and desire to secure by the Letters PATENT is:

1. A method of forming a sub-0.1 μm channel length MOSFET which comprises the steps of:

forming a planar structure comprising a Si-containing substrate, a sacrificial oxide layer located atop a surface of said Si-containing substrate, a patterned polysilicon region located atop a portion of said sacrificial oxide layer and a dielectric material abutting said patterned polysilicon region;

removing said patterned polysilicon region to provide an opening exposing a portion of said sacrificial oxide layer and implanting ions into said Si-containing substrate to form a device channel/body implant region, said device channel/body implant region having a length less than 0.1 μm;

forming Si spacers on exposed vertical sidewalls of said dielectric material;

removing said exposed portion of sacrificial oxide layer utilizing a chemical oxide removal etch to expose a surface of said Si-containing substrate;

forming a gate dielectric on the exposed surface of said Si-containing substrate and oxidizing said Si spacers;

forming a recessed poly-gate region in said gate dielectric, said recessed poly-gate having an oxide layer on an upper surface thereof;

laterally etching said oxidized Si spacers and portions of said dielectric material which are above said recessed poly-gate to provide an area which is wider than said recessed poly-gate;

forming a gate conductor in said area and removing remaining dielectric material; and

forming nitride spacers on exposed vertical sidewalls of said recessed poly-gate that are beneath said gate conductor.

2. The method of Claim 1 wherein said patterned polysilicon region is removed by chemical downstream etching or a KOH etching process.

3. The method of Claim 1 wherein said Si spacers are formed by deposition and etching.

4. The method of Claim 1 wherein said chemical oxide removal etch is conducted in the presence of a vapor containing HF and NH_3.

5. The method of Claim 1 wherein said chemical oxide removal etch is conducted in a plasma containing HF and NH_3.

6. The method of Claim 1 wherein said gate dielectric is an oxide which is formed by a thermal growing process.

7. The method of Claim 1 wherein said Si spacers are oxidized during formation of said gate dielectric.

8. The method of Claim 1 wherein said lateral etching is performed utilizing a chemical oxide removal etch.

9. The method of Claim 8 wherein said chemical oxide removal etch is conducted in the presence of a vapor containing HF and NH_3.

10. The method of Claim 8 wherein said chemical oxide removal etch is conducted in a plasma containing HF and NH_3.

11. A method of selectively removing an oxide layer from a structure, said method comprising the steps of:

providing a semiconductor structure containing at least an oxide layer; and

selectively removing portions of said oxide layer utilizing a chemical oxide removal etch which is conducted in the presence of a plasma containing HF and NH_3.

12. The method of Claim 11 wherein said chemical oxide removal etch is performed at a pressure of about 6 millitorr or below.

13. The method of Claim 11 wherein said chemical oxide removal etch results in an undercut region being formed in said structure.

14. A low-resistance T-gate MOSFET comprising

a Si-containing substrate comprising at least one device channel/body implant region separating a source region from a drain region, said at least one device channel/body implant region having a length of less than about 0.1 μm;

a gate dielectric located at least atop said device channel/body implant region, said source region and said drain region;

a T-gate located atop a portion of said gate dielectric, said T-gate comprises a recessed bottom polysilicon region and an upper gate conductor region, said upper gate conductor region has a width that is greater than a width of said bottom polysilicon region; and

nitride spacers located on exposed vertical sidewalls of said bottom polysilicon region, said nitride spacers have an outer edge that is aligned with an outer edge of the upper gate conductor region.

15. The low-resistance T-gate MOSFET of Claim 14 wherein said gate dielectric is an oxide having a dielectric constant of about 3.0 or greater.

16. The low-resistance T-gate MOSFET of Claim 14 wherein said Si-containing substrate is a component of a silicon-on-insulator wafer.

17. The low-resistance T-gate MOSFET of Claim 14 wherein said upper gate conductor is composed of polysilicon, a conductive metal, a silicide or a combination thereof.

18. The low-resistance T-gate MOSFET of Claim 17 wherein said upper gate conductor is composed of a conductive metal.

19. The low-resistance T-gate MOSFET of Claim 14 wherein said upper gate conductor is composed of W.

20. The low-resistance T-gate MOSFET of Claim 14 wherein said upper gate conductor is comprised of a conductive stack including W located atop polySi.